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EXAMINER				
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ART UNIT		PAPER NUMBER		
2813				
NOTIFICATION DATE		DELIVERY MODE		
05/26/2010		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/576,416

Applicant(s)

NAITO ET AL.

Examiner

LATANYA CRAWFORD

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14-24 is/are rejected.
- 7) ☒ Claim(s) 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 December 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the correspondence filed on 2/04/2010.

Currently, claims 1-24 are pending.

Drawings

2. The drawings were received on 12/22/2009. These drawings are acceptable.

Claim Objections

3. Claim 1 is objected to because of the following informalities: It is unclear if there is more than one semiconductor layer. If applicant is only referring to one semiconductor layer, there is no antecedent basis for "a semiconductor layer" line 9, pp. 2. To further prosecution, Examiner interprets that there is only one semiconductor layer. Appropriate correction is required.

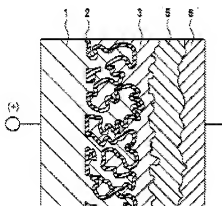
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-12, 14-21, & 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida (US Pub no. 2003/0133256 A1).



Regarding claim 1, Yoshida et al. discloses (fig. 1) a method for producing a capacitor comprising, as one electrode (anode), an electric conductor (1) having pores and having formed on the surface thereof a dielectric layer (2) and, as the other electrode (cathode) [0035], a semiconductor layer (3) formed on the electric conductor by energization in a semiconductor layer-forming electrolytic solution, the method comprising impregnating the pores of the electric conductor with a semiconductor layer-forming precursor before energization [0060] to render the concentration of semiconductor layer-forming precursor in the pores higher than that of semiconductor layer-forming precursor in the electrolytic solution (the limitation: to render.... Is the intended result of a process step positively recited)[0060], immersing the impregnated electric conductor (3) into the electrolytic solution, and passing an electric current through the electrolytic solution to form a semiconductor layer on the impregnated electric conductor [0058-0060].

Regarding claim 2, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the electrolytic solution (phosphoric acid) is an electrolytic solution not containing a semiconductor layer-forming precursor [0060].

Regarding claim 3, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the electric conductor is at least one member selected from a metal [0035].

Regarding claim 4, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the electric conductor is a laminated body having, as the surface layer, at least one member selected from a metal (lead/conductor) [0064].

Regarding claim 5, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 3, wherein the electric conductor is a metal or alloy mainly comprising at least one member selected from tantalum, niobium and aluminum [0035].

Regarding claim 6, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the electric conductor is tantalum having a CV value of 100,000 gF.V/g or more [0035][0070].

Regarding claim 7, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the electric conductor is niobium having a CV value of 150,000 gF.V/g or more [0035][0070].

Regarding claim 8, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the electric conductor has a size of 5 mm³ or more [0059].

Regarding claim 9, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the electric conductor has a foil shape and the depth of pore formed by etching is 200 µm or more [0059].

Regarding claim 10, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the dielectric layer mainly comprises at least one member selected from metal oxides such as Ta_2O_5 [0059]

Regarding claim 11, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the semiconductor layer-forming precursor is at least one member selected from an a thiophene derivative (raw material of polythiophene), and a pyrrole derivative (raw material of polypyrrole or polymethylpyrrole) [0060][0081].

Regarding claim 12, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 11, wherein the semiconductor layer-forming precursor is pyrrole or 3,4-ethylenedioxythiophene [0060][0081].

Regarding claim 14, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 1, wherein the semiconductor layer is at least one member selected from an organic semiconductor layer and an inorganic semiconductor layer [0037-0038].

Regarding claim 15, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 14, wherein the organic semiconductor is at least one member selected from an organic semiconductor mainly comprising tetracyano-quinodimethane[0038].

Regarding claim 16, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 15, wherein the electrically conducting polymer containing a

repeating unit represented by formula (1) is an electrically conducting polymer containing a structure unit represented by the following formula (3) as a repeating unit:

wherein R^6 and R^7 each independently represents a hydrogen atom, a linear or branched, saturated or unsaturated alkyl group having from 1 to 6 carbon atoms, or a substituent for forming at least one 5-, 6- or 7-membered saturated hydrocarbon cyclic structure containing two oxygen atoms when the alkyl groups are combined with each other at an arbitrary position, and the cyclic structure includes a structure having a vinylene bond which may be substituted, and a phenylene structure which may be substituted [0037].

Regarding claim 17, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 16, wherein the electrically conducting polymer is selected from polyaniline, polythiophene, poly-pyrrole, and substitution derivatives and copolymers thereof [0037].

Regarding claim 18, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 17, wherein the electrically conducting polymer is poly(3,4-ethylenedioxythiophene) [0037].

Regarding claim 19, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 14, wherein the inorganic semiconductor is at least one compound selected from manganese dioxide [0038].

Regarding claim 20, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 14, wherein the electrical conductivity of the semiconductor is from 10^{-2} to 10^3 S/cm [0004].

Regarding claim 21, Yoshida et al. discloses a capacitor produced by the production method claimed in claim 1 (fig.1).

Regarding claim 23, Yoshida et al discloses an electronic circuit using the capacitor claimed in claim 21 [0002][0058-0060].

Regarding claim 24, Yoshida et al. discloses an electronic device using the capacitor claimed in claim 21 [0002][0058-0060].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (US Pub no. 2003/0133256 A1).

Regarding claim 22, Yoshida et al discloses all the claim limitations of claim 21 and further teaches impregnation ratio[0032]but fails to teach an impregnation ratio of the semiconductor is 90% or more. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the impregnation ratio of the semiconductor is 90% or more would result since Yoshida et al. teaches substantially identical

structures (in view of recently submitted drawings compared to Yoshida et al. fig. 1), and substantially identical processes a prima facie case of obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Allowable Subject Matter

7. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LATANYA CRAWFORD whose telephone number is (571)270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571)-272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LaTanya Crawford/
Examiner, Art Unit 2813

/W. David Coleman/
Primary Examiner, Art Unit 2823